WHAT IS CLAIMED IS:

1. A replica network that controls a resistance of a signal conducting MOSFET switch in a switched capacitor circuit, comprising:

a bridge circuit, wherein a MOSFET resistor is disposed in a resistor branch of said bridge circuit; and

an operational amplifier, wherein a noninverting terminal of said operational amplifier is connected to a first node of said bridge circuit, an inverting terminal of said operational amplifier is connected to a second node of said bridge circuit, said second node is separated from said first node by a third node of said bridge circuit, an output of said operational amplifier is connected to a gate terminal of said MOSFET resistor and to a gate terminal of the signal conducting MOSFET switch to control the resistance of the signal conducting MOSFET switch.

2. The replica network of claim 1, further comprising a compensation capacitor connected in parallel between said output of said operational amplifier and said second node.

3. The replica network of claim 1, further comprising an analog ground connection to said third node of said bridge circuit.

4. The replica network of claim 1, further comprising a voltage input signal connection to a fourth node of said bridge circuit.

5. The replica network of claim 1, wherein a resistance of a first resistor connected between said first node and said third node of said bridge circuit equals a resistance of a second resistor connected between said second node and said third node.

6. The replica network of claim 5, wherein said MOSFET resistor is connected between said second node and a fourth node of said bridge circuit.

7. The replica network of claim 6, wherein the resistance of a third resistor connected between said first node and said fourth node is smaller than the resistance of said first resistor.

8. The replica network of claim 7, wherein said output of said operational amplifier controls the resistance of said MOSFET resistor so that the resistance of said MOSFET resistor equals the resistance of said third resistor.

9. The replica network of claim 7, wherein said output of said operational amplifier controls the resistance of the MOSFET switch so that the resistance of the signal conducting MOSFET switch equals the resistance of said third resistor.

10. The replica network of claim 1, wherein said MOSFET resistor is connected between said second node and a fourth node of said bridge circuit.

11. The replica network of claim 1, wherein the resistance of a third resistor connected between said first node and a fourth node is smaller than the resistance of a first resistor connected between said first node and said third node.

12. The replica network of claim 1, wherein said output of said operational amplifier controls the resistance of said MOSFET resistor so that the resistance of said MOSFET resistor equals the resistance of a third resistor connected between said first node and a fourth node.

13. The replica network of claim 1, wherein said output of said operational amplifier controls the resistance of the MOSFET switch so that the resistance of

the signal conducting MOSFET switch equals the resistance of a third resistor connected between said first node and a fourth node.

14. The replica network of claim 1, wherein said MOSFET resistor has a threshold voltage less than or equal to zero volts.

15. The replica network of claim 14, wherein said MOSFET resistor is a native NMOSFET device.

16. The replica network of claim 1, wherein said MOSFET resistor is the same type and size as the signal conducting MOSFET switch.

17. The replica network of claim 1, further comprising a first switch disposed within the connection between said output of said operational amplifier and the gate terminal of the signal conducting MOSFET switch.

18. The replica network of claim 17, wherein said first switch cycles to an open state and a closed state in response, respectively, to an off state and an on state of a first clock waveform.

19. The replica network of claim 18, further comprising a second switch connected between a fifth node and analog ground, wherein said fifth node is disposed within the connection between said first switch and the gate terminal of the signal conducting MOSFET switch.

20. The replica network of claim 19, wherein said second switch cycles to an open state and a closed state in response, respectively, to an off state and an on state of a second clock waveform.

21. A replica network that controls a resistance of a signal conducting MOSFET switch in a switched capacitor circuit, comprising:

means to connect a voltage input signal to a bridge circuit and to the switched capacitor circuit;

means to regulate a gate voltage of a MOSFET resistor disposed in a resistor branch of said bridge circuit to control a resistance of said MOSFET resistor; and

means to connect said regulated gate voltage to a gate terminal of the signal conducting MOSFET switch in the switched capacitor circuit, thereby controlling the resistance of the signal conducting MOSFET switch.

22. A switched capacitor circuit, comprising:

an integrator;

a summing junction switch connected to said integrator;

a sampling capacitor connected to said summing junction switch;

a signal conducting MOSFET switch connected to said sampling capacitor; and

a replica network that controls a resistance of said signal conducting MOSFET switch, said replica network connected to a gate terminal of said signal conducting MOSFET switch.

23. The switched capacitor circuit of claim 22, wherein said integrator is a differential integrator and said summing junction switch is connected to an inverting terminal of said differential integrator.

24. The switched capacitor circuit of claim 23, further comprising:

a second summing junction switch connected to a noninverting terminal of said differential integrator;

a second sampling capacitor connected to said second summing junction switch;

a second signal conducting MOSFET switch connected to said second sampling capacitor; and

a second replica network that controls the resistance of said second signal conducting MOSFET switch connected to a gate terminal of said second signal conducting MOSFET switch.

25. A method for reducing track mode distortion in a switched capacitor circuit, comprising the steps of:

(1) connecting a voltage input signal to a first node of a bridge circuit and to the switched capacitor circuit;

(2) regulating a gate voltage of a MOSFET resistor disposed in a resistor branch of the bridge circuit to control the resistance of the MOSFET resistor; and

(3) connecting said regulated gate voltage to a gate terminal of a signal conducting MOSFET switch in the switched capacitor circuit, thereby controlling the resistance of the signal conducting MOSFET switch so that it is independent of the voltage input signal, thereby reducing track mode distortion in the switched capacitor circuit.

26. The method of claim 25, wherein the MOSFET resistor is the same type and size as the signal conducting MOSFET switch.

27. The method of claim 25, wherein step (2) comprises the steps of:

(a) connecting a noninverting terminal of an operational amplifier to a second node of the bridge circuit and an inverting terminal of the operational amplifier to a third node of the bridge circuit, wherein the third node is separated from the second node by the first node; and

(b) connecting an output of the operational amplifier to a gate terminal of the MOSFET resistor, thereby regulating the gate voltage of the MOSFET

resistor disposed in the resistor branch of the bridge circuit to control the resistance of the MOSFET resistor.

28. The method of claim 27, further comprising the step of:

(c) connecting a compensation capacitor in parallel between the output of the operational amplifier and the third node.

29. The method of claim 27, wherein the MOSFET resistor is connected between the first node and the third node.

30. The method of claim 29, wherein the output of the operational amplifier controls the resistance of the MOSFET resistor so that the resistance of the MOSFET resistor equals the resistance of a resistor connected between the first node and the second node.

31. The method of claim 29, wherein the output of the operational amplifier controls the resistance of the signal conducting MOSFET switch so that the resistance of the signal conducting MOSFET switch equals the resistance of a resistor connected between the first node and the second node.

32. A method for reducing signal distortion due to charge injection from a summing junction switch in a switched capacitor circuit, comprising the steps of:

(1) connecting a voltage input signal to a first node of a bridge circuit and to the switched capacitor circuit;

(2) regulating a gate voltage of a MOSFET resistor disposed in a resistor branch of the bridge circuit to control the resistance of the MOSFET resistor; and

(3) connecting said regulated gate voltage to a gate terminal of a signal conducting MOSFET switch in the switched capacitor circuit, thereby controlling the resistance of the signal conducting MOSFET switch so that it is

independent of the voltage input signal, thereby reducing signal distortion due to charge injection from the summing junction switch in the switched capacitor circuit.

33. The method of claim 32, wherein the MOSFET resistor is similar to as the signal conducting MOSFET switch.

34. The method of claim 32, wherein step (2) comprises the steps of:

(a) connecting a noninverting terminal of an operational amplifier to a second node of the bridge circuit and an inverting terminal of the operational amplifier to a third node of the bridge circuit, wherein the third node is separated from the second node by the first node; and

(b) connecting an output of the operational amplifier to a gate terminal of the MOSFET resistor, thereby regulating the gate voltage of the MOSFET resistor disposed in the resistor branch of the bridge circuit to control the resistance of the MOSFET resistor.

35. The method of claim 34, further comprising the step of:

(c) connecting a compensation capacitor in parallel between the output of the operational amplifier and the third node.

36. The method of claim 34, wherein the MOSFET resistor is connected between the first node and the third node.

37. The method of claim 36, wherein the output of the operational amplifier controls the resistance of the MOSFET resistor so that the resistance of the MOSFET resistor equals the resistance of a resistor connected between the first node and the second node.

38. The method of claim 36, wherein the output of the operational amplifier controls the resistance of the signal conducting MOSFET switch so that the resistance of the signal conducting MOSFET switch equals the resistance of a resistor connected between the first node and the second node.